REMARKS

This submission with RCE is in response to the Final Action mailed November 30, 2006. Claims 29, 31-33, 35 and 36 were examined. With the present submission, claims 29 and 33 are being amended.

Rejection Under 35 USC 102(e) of Claim 29

1. Claim 29 is rejected under 35 U.S.C. 102(e) as being unpatentable over U.S. Pat. No. 6,433,842 to Kaneko. Claim 29 is an independent claim, on which claims 31 and 32 depend. Applicant submits that claim 29 is patentable for the reasons discussed below, together with claims 31 and 32, at least by virtue of their dependency on claim 29.

2. The Examiner asserts that Kaneko teaches a thin film transistor (Fig. 1) comprising first and second sacrifice layers (8) with island shapes respectively formed on the source doped silicon layer (6) and drain doped silicon layer (6) in their entirety, the first and the second sacrifice layers being spaced apart by the channel and further spaced from the insulating layer (4) in their entirety.

3. However, claim 29 recites *"first and second sacrifice layers . . . wherein an entire bottom of the first and second sacrifice layers is higher than a top of the semiconductor layer."* To the contrary, as disclosed by Kaneko in Fig. 1, the alloy layer (8) is formed over the semiconductor layer (5), and **a portion of a bottom of the alloy layer (8) is lower than a top of the semiconductor layer (5).** It is clear that the bottom of the alloy layer (8) in Kaneko is not entirely higher than the top of the semiconductor layer (5). Therefore, the thin film transistor as recited in claim 29 is not anticipated by Kaneko, because the bottom of Kaneko's alloy layer (8) is not entirely higher than the top of Kaneko's semiconductor layer (5).

4. In view of the above, Applicant respectfully submits that claim 29 is novel over Kaneko, together with claims 31 and 32, at least by virtue of their dependence on claim 29.

Rejection Under 35 USC 102(b) of claim 33

1. Claim 33 is rejected under 35 USC 102(b) as being unpatentable over U.S. Pat. No. 5,726,641 to Shimada. Claim 33 is an independent claim, on which claims 35 and 36 depend. Applicant submits that claim 33 is patentable for the reasons discussed below, together with claims 35 and 36, at least by virtue of their dependency on claim 33.

2. The Examiner asserts that Shimada teaches a thin film transistor (Fig. 7) comprising first and second sacrifice layers (15) with island shapes formed over and in direct contact with the semiconductor layer (13) in their entirety, and a channel being defined between the first and second sacrifice layers (region between 15) so as to expose the semiconductor layer (13).

3. Claim 33 recites a thin film transistor comprising a semiconductor layer, a source doped silicon layer and a drain doped silicon layer "*wherein the source doped silicon layer and the drain doped silicon layer are in contact with the semiconductor layer.*" In stark contrast, as disclosed by Shimada in Fig. 7, the amorphous n+ silicon layer (25) is formed on the micro-crystalline n+ silicon layer (15) which, in turn, is formed on the semiconductor layer (13). Therefore, **the amorphous n+ silicon layer (25) does not contact the semiconductor layer (13).** As a consequence, reconsideration of the Examiner's rejection is respectfully requested.

4. Applicant submits that amended claim 33 is allowable Shimada, together with claims 35 and 36, at least by virtue of their dependency on claim 33.

* * *

In view of the above, reconsideration and allowance of all the claims are respectfully solicited.

The Commissioner is authorized to charge any additional fees, which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 on

February 22, 2007
(Date of Transmission)

Diane Osollo
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Feb. 22, 2007
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